RELIABILITY EVALUATION REPORT STATUS AND FORECAST

for SiC MOSFET 1200V Transfer from Catania 4" to Catania 6"

General Information	
Commercial Product	*: SCTWA50N120/SCT30N120H _SCT30N120*
Product Line (Test Vehicle)	*: K12B01/C12B01*
Product Description	*:* SiC Power MOSFET
Package	*: HIP247LL /H2PAK/HIP247*
Silicon Technology	*:* Silicon Carbide MOSFET GEN1
Division	*: Power Transistor Division*

Traceability	
Diffusion Plant	*:* CT 6" (Catania Italy)
Assembly Plant	*: SC PSI LAGUNA – (Philippines) / STS SHENZHEN (China)*

Reliability Assessment	
Passed	☒
Failed	☐

Disclaimer: *this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)*

REVISION HISTORY

Version	Date	Author	Changes description
1.0	21 February 2018	A.SETTINIERI	Preliminary Report
2.0	12 March 2018	A.SETTINIERI	Second issue

APPROVED BY:

Corrado CAPPELLO
ADG Q&R department - Catania
ST Microelectronics

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1. RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Reliability evaluation for Silicon Carbide technology transfer from 4inch Catania fab to CT6" Catania fab.

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with JEDEC and internal spec 0061692 specification and are listed in the Test Plan.
For details on test conditions, generic data used and spec reference see test results summary at Par.3

#	Stress	Abrv	Reference	Test Flag	Comments
1	Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	Y	
2	Pre-conditioning	PC	JESD22A-113	Y	
3	External Visual	EV	JESD22B-101	Y	
4	High Temperature Gate Bias	HTGB	JESD22A-108	Y	
5	High Temperature Reverse Bias	HTRB	JESD22A-108	Y	
6	ESD Characterization	ESD (HBM, CDM)	ESDA-JEDEC JES-001 and AINSI-ESD S5.3.1	Y	
7	Autoclave	AC	JESD22A-102	Y	
8	High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	Y	
9	Temperature Cycling	TC	JESD22A-104	Y	
10	Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	Y	

1.3 PRELIMINARY Conclusion

All reliability preliminary tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die and package oriented test showed a good stability of the main electrical monitored parameters.

2. DEVICE/TEST VEHICLE CHARACTERISTICS

2.1 Generalities

SiC MOSFET Gen1

2.2 Traceability

Reference “Product Baseline” document if existing, else provide following chapters/information:

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	CT 6” (Catania - Italy)
Wafer diameter (inches)	6”
Silicon process technology	SiC MOSFET Gen1
Die finishing front side (passivation)	Polymide
Die finishing back side	Ti-Ni-Au
Die area (Stepping die size)	4000 x 4000 µm^2 (K12B) 3800 x 3800 µm^2 (C12B)
Metal levels/Materials	Al-Si-Cu

Assembly information

Assembly Information	
Assembly plant location	*SC PSI* LAGUNA – (Philippines) / STS SHENZHEN (China)
Package code description	HIP247-Long Lead / H2PAK / HiP247
Leadframe/Substrate	TO247 #DWG LF0009800 Full Ni with groove (HIP247-LL) D2PAK 3L Mon HC Ve1 SelNi/NiP (H2PAK) TO247 3L Mon Ve6 OpA/Q SelNi/NiP (HIP247)
Die attach material	Soft Solder Die Attach SnAgSb (K12B) PREFORM Pb/Ag/Sn (C12B)
Wires bonding materials/diameters	Al
Molding compound	Halogen Free

Reliability testing information

Reliability Testing Information	
Reliability laboratory location	Catania (Italy)
Electrical testing location	Catania (Italy)

3. TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	Commercial Product	Product lines	Package	Wafer Fab	Assembly plant	Note
1	SCTWA50N120	K12B01	HIP247-LL	CT 6”	SC PSI LAGUNA (Philippines)	
2	SCT30N120H	C12B01	H2PAK		STS SHENZHEN (China)	
3	SCT30N120		HIP247			

3.2 Test results summary

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S)	Steps	Failure/SS		
							Lot 1	Lot 2	Lot 3
1	**TEST**		User specification	All qualification parts tested per the requirements of the appropriate device specification.			235	235	235
2	**External visual**		JESD22 B-101	All devices submitted for testing			235	235	235
Silicon Oriented Tests									
3	**HTRB**	N	JESD22 A-108	Ta=200°C ; BIAS= 960V	135	168H	0/45	Wk 18/2018	0/45
						500H	0/45		0/45
						1000H	0/45		Wk 13/2018
4	**HTGB 1**	N	JESD22 A-108	Ta=200°C ; BIAS= 20V	135	168H	0/45	Wk 18/2018	0/45
						500H	0/45		0/45
						1000H	0/45		Wk 13/2018
5	**HTGB 2**	N	JESD22 A-108	Ta=200°C ; BIAS= -10V	135	168H	0/45	Wk 18/2018	0/45
						500H	0/45		0/45
						1000H	0/45		WK 13/2018
Package Oriented Tests									
6	**Pre-conditioning**		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C,RH=85% IR Reflow @ 245°C 3 times	All devices to be subjected to H3TRB, TC, AC, IOL	Final		Wk 15/2018	
7	**AC**	Y	JESD22 A-102	Ta=121°C , P=2atm	75	96H	0/25	Wk 16/2018	0/25
8	**H3TRB**	Y	JESD22 A-101	Ta=85°C , RH=85% , Vbias=100V	75	168H	0/25	Wk 21/2018	0/25
						500H	0/25		0/45
						1000H	0/25		Wk 13/2018
9	**TC**	Y	JESD22 A-103	Ta= –65°C / +150°C (1h cycle - 30min at extreme temp.)	75	100Cy	0/25	WK 21/2018	0/25
						200Cy	0/25		0/25
						500Cy	0/25		WK 13/2018
10	**IOL/TF**	Y	MIL-STD 750D Method 1037	ΔTj ≥ 100°C	75	5Kcy	0/25	Wk 19/2018	0/25
						10Kcy	0/25		0/25
11	**ESD**		ESDA-JEDEC_ JES-001 ANSI-ESD S5.3.	HBM CDM	3		0/3		

Automotive Discrete Group (ADG)
Power Transistor Division

Process Change Notification

SiC MOSFET 1200V Gen1 Transfer from Catania 4” to Catania 6”

Dear Customer,

Following the continuous improvement of our service and in order to increase productivity, we are pleased to announce that *SiC MOSFET 1200V Gen 1* technology wafers, currently manufactured in Catania 4 inch FAB, will be performed in Catania 6 inch FAB.
Wafers produced in Catania 6 inch FAB, guarantee the same quality and electrical characteristics as per current production.

In the next pages, we are reporting the qualification plan to reach full maturity.

The change has been classified as **Class 1** according to the ZVEI and ST internal rules.

	Assessment of impact on Supply Chain regarding following aspects - contractual agreements - technical interface of processability / manufacturability of customer - form, fit, function, quality performance, reliability	**Remaining risks on Supply Chain?**	
ID	**Type of change**	**No**	**Yes**
SEM-PW-02	New wafer diameter	**P**	**P**
SEM-PW-03	New final wafer thickness	**P**	**P**

The qualification of the change will be completed according the qualification plan reported in the following pages; the first results are reported in the attached file

Sincerely Yours!

<table>
<tr><td colspan="2">Tech name
SiC MOSFET 1200V Transfer from Catania 4” to Catania 6”</td></tr>
<tr><td>ST Part number:</td><td>ST PNs: Catania 6 inch FAB
Package: All the Packages</td></tr>
<tr><td>Reason and background of the change</td><td>To increase flexibility and increase Capacity</td></tr>
<tr><td>Detailed description of change(s), including affected type of changes</td><td>The Diffusion Process Catania 4 inch, will be performed in Catania 6 inch FAB.</td></tr>
<tr><td>Impact on form, fit, function, or reliability.</td><td>No Impact</td></tr>
<tr><td>Datasheet</td><td>No Impact – No Change</td></tr>
<tr><td>Benefit of the change</td><td>Capacity and flexibility increase.</td></tr>
<tr><td>Qualification Plan and Implementation date for change</td><td>
<table>
<tr><th>Test Vehicles</th><th>N. of Lots</th><th>Reliability Plan</th><th>Parametric Verification</th><th>Forecast (wk)</th></tr>
<tr><td>SCTWA50N120</td><td>1</td><td rowspan="3">JEDEC Compliant & ST spec 0061692</td><td>X</td><td>DONE</td></tr>
<tr><td>SCT30N120H</td><td>1</td><td>X</td><td>21/2018</td></tr>
<tr><td>SCT30N120</td><td>1</td><td>X</td><td>13/2018</td></tr>
</table>

Planned Implementation Date → wk 21 2018</td></tr>
<tr><td>Traceability Info</td><td>By QA Number</td></tr>
<tr><td>PPAP Update</td><td>NA</td></tr>
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